Amendments to the Claims

Listing of claims

Claims 1-13 (cancelled)

Claim 14 (currently amended): An apparatus for adjusting a phase difference between two input signals, the apparatus comprising:

a first buffer for buffering a first input signal and outputting a first output signal;

a first DAC for outputting a first control voltage corresponding to a first digital value representative of a phase delay;

a first variable capacitor coupled to the first DAC and the first buffer, the capacitance value of the first variable capacitor corresponding to the first control voltage;

a second buffer for buffering a second input signal and outputting a second output signal;

a second DAC for outputting a second control voltage corresponding to a second digital value representative of a phase delay; and

a second variable capacitor coupled to the second DAC and the second buffer, the capacitance value of the second variable capacitor corresponding to the second control voltage;

wherein by controlling at least one of the first and the second digital values, the phase difference between the first input signal and the second input signal is adjusted, and the first input signal and the second input signal are differential signals.

Claim 15 (previously presented): The apparatus of claim 14 being implemented in a receiver.

Claim 16 (previously presented): The apparatus of claim 14 being implemented in a transmitter.

Claim 17 (previously presented): The apparatus of claim 14 being implemented in a transceiver.

Claim 18-19 (cancelled)

Claim 20 (previously presented): The apparatus of claim 14, wherein the first input signal and the second input signals are clock signals.

Claim 21 (previously presented): The apparatus of claim 14, wherein the first input signal and the second input signal are RF signals.

Claim 22 (previously presented): The apparatus of claim 14, wherein the first variable capacitor and the second variable capacitor are voltage-controlled capacitors.

Claim 23 (previously presented): The apparatus of claim 22, wherein the voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

Claim 24 (previously presented): The apparatus of claim 22, wherein the voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.

Claim 25 (currently amended): A method for adjusting a phase difference between two input signals, the method comprising:

buffering a first input signal and outputting a first output signal;

buffering a second input signal and outputting a second output signal;

providing at least one of a first digital value and a second digital value

representative of a first phase delay and a second phase delay respectively; and

adjusting at least one of a capacitance value of a first variable capacitor with a first control voltage generated from the first digital value and a capacitance value of a second variable capacitor with a second control voltage generated from the second digital value, to adjust the phase difference between the input signal and the output signal;

wherein the first input signal and the second input signal are differential signals.

Claim 26 (cancelled)

Claim 27 (previously presented): The method of claim 25, wherein the first input signal and the second input signal are an in-phase signal and a quadrature-phase signal respectively.

Claim 28 (previously presented): The method of claim 25, wherein the first input signal and the second input signals are clock signals.

Claim 29 (previously presented): The method of claim 25, wherein the first input signal and the second input signal are RF signals.

Claim 30 (previously presented): The method of claim 25, wherein the first variable capacitor and the second variable capacitor are voltage-controlled capacitors.

Claim 31 (previously presented): The method of claim 30, wherein the voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

Claim 32 (previously presented): The method of claim 30, wherein the

voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.

Claim 33 (previously presented): An apparatus for adjusting a phase difference between an in-phase signal and a quadrature-phase signal, the apparatus comprising:

a first adjusting circuit, the first adjusting circuit comprising:

a first buffer for buffering the in-phase signal and outputting a first output signal;

a first DAC for outputting a first control voltage corresponding to a first digital value representative of a phase delay; and

a first variable capacitor coupled to the first DAC and the first buffer, the capacitance value of the first variable capacitor corresponding to the first control voltage; and

a second adjusting circuit, the second adjusting circuit comprising:

a second buffer for buffering the quadrature-phase signal and outputting a second output signal;

a second DAC for outputting a second control voltage corresponding to a second digital value representative of a phase delay; and

a second variable capacitor coupled to the second DAC and the second buffer, the capacitance value of the second variable capacitor corresponding to the second control voltage;

wherein by controlling at least one of the first and the second adjusting circuit, the phase difference between the in-phase signal and the quadrature-phase signal reaches a predetermined condition.

Claim 34 (previously presented): An apparatus for adjusting a phase difference between a positive signal of a differential signal and a negative signal of the differential signal, the apparatus comprising:

a first adjusting circuit, comprising:

a first buffer for buffering the positive signal and outputting a first output signal;

a first DAC for outputting a first control voltage corresponding to a first digital value representative of a phase delay; and

a first variable capacitor coupled to the first DAC and the first buffer, the capacitance value of the first variable capacitor corresponding to the first control voltage; and

a second adjusting circuit, comprising:

a second buffer for buffering the negative signal and outputting a second output signal;

a second DAC for outputting a second control voltage corresponding to a second digital value representative of a phase delay; and

a second variable capacitor coupled to the second DAC and the second buffer, the capacitance value of the second variable capacitor corresponding to the second control voltage;

wherein by controlling at least one of the first and the second adjusting circuit, the phase difference between the positive signal and the negative signal reaches a predetermined condition.

Claim 35 (previously presented): A method for adjusting a phase difference between an in-phase signal and a quadrature-phase signal, the method comprising:

buffering the in-phase signal and outputting a first output signal;

buffering the quadrature-phase signal and outputting a second output signal;

providing at least one of a first digital value and a second digital value representative of a first phase delay and a second phase delay respectively; and

adjusting at least one of a first variable capacitor and a second variable capacitor by respectively utilizing a first control voltage generated from

the first digital value and a second control voltage generated from the second digital value, to have the phase difference between the in-phase signal and the quadrature-phase signal reach a predetermined condition.

Claim 36 (previously presented): A method for adjusting a phase difference between a positive signal of a differential signal and a negative signal of the differential signal, the method comprising:

buffering the positive signal and outputting a first output signal;

buffering the negative signal and outputting a second output signal;

providing at least one of a first digital value and a second digital value representative of a first phase delay and a second phase delay respectively; and

adjusting at least one of a first variable capacitor and a second variable capacitor by respectively utilizing a first control voltage generated from the first digital value and a second control voltage generated from the second digital value, to have the phase difference between the positive signal and the negative signal reach a predetermined condition.

Claim 37 (previously presented): The apparatus of claim 33 being implemented in a receiver.

Claim 38 (previously presented): The apparatus of claim 33 being implemented in a transmitter.

Claim 39 (previously presented): The apparatus of claim 33 being implemented in a transceiver.

Claim 40 (previously presented): The apparatus of claim 33, wherein the in-phase signal and the quadrature-phase signal are RF signals.

Claim 41 (previously presented): The apparatus of claim 33, wherein the first variable capacitor and the second variable capacitor are voltage-controlled capacitors.

Claim 42 (previously presented): The apparatus of claim 41, wherein the voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

Claim 43 (previously presented): The apparatus of claim 41, wherein the voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.

Claim 44 (previously presented): The apparatus of claim 34 being implemented in a receiver.

Claim 45 (previously presented): The apparatus of claim 34 being implemented in a transmitter.

Claim 46 (previously presented): The apparatus of claim 34 being implemented in a transceiver.

Claim 47 (previously presented): The apparatus of claim 34, wherein the positive signal and the negative signal are clock signals.

Claim 48 (previously presented): The apparatus of claim 34, wherein the first variable capacitor and the second variable capacitor are voltage-controlled capacitors.

Claim 49 (previously presented): The apparatus of claim 48, wherein the voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

Claim 50 (previously presented): The apparatus of claim 48, wherein the voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.

Claim 51 (previously presented): The method of claim 35, wherein the in-phase signal and the quadrature-phase signal are RF signals.

Claim 52 (previously presented): The method of claim 36, wherein the positive signal and the negative signal are clock signals.

Claim 53 (new): An apparatus for adjusting a phase difference between two input signals, the apparatus comprising:

a first buffer for buffering a first input signal and outputting a first output signal;

a first DAC for outputting a first control voltage corresponding to a first digital value representative of a phase delay;

a first variable capacitor coupled to the first DAC and the first buffer, the capacitance value of the first variable capacitor corresponding to the first control voltage;

a second buffer for buffering a second input signal and outputting a second output signal;

a second DAC for outputting a second control voltage corresponding to a second digital value representative of a phase delay; and

a second variable capacitor coupled to the second DAC and the second buffer, the capacitance value of the second variable capacitor corresponding to the second control voltage;

wherein by controlling at least one of the first and the second digital values, the phase difference between the first input signal and the second input signal is adjusted, and the first input signal and the second input signal are an in-phase signal and a

quadrature-phase signal respectively.

Claim 54 (new): The apparatus of claim 53 being implemented in a receiver.

Claim 55 (new): The apparatus of claim 53 being implemented in a transmitter.

Claim 56 (new): The apparatus of claim 53 being implemented in a transceiver.

Claim 57 (new): The apparatus of claim 53, wherein the first input signal and the second input signal are differential signals.

Claim 58 (new): The apparatus of claim 53, wherein the first input signal and the second input signals are clock signals.

Claim 59 (new): The apparatus of claim 53, wherein the first input signal and the second input signal are RF signals.

Claim 60 (new): The apparatus of claim 53, wherein the first variable capacitor and the second variable capacitor are voltage-controlled capacitors.

Claim 61 (new): The apparatus of claim 60, wherein the voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

Claim 62 (new): The apparatus of claim 60, wherein the voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.

Claim 63 (new): A method for adjusting a phase difference between two input signals, the method comprising:

buffering a first input signal and outputting a first output signal;

buffering a second input signal and outputting a second output signal;

providing at least one of a first digital value and a second digital value representative of a first phase delay and a second phase delay respectively; and

adjusting at least one of a capacitance value of a first variable capacitor with a first control voltage generated from the first digital value and a capacitance value of a second variable capacitor with a second control voltage generated from the second digital value, to adjust the phase difference between the input signal and the output signal;

wherein the first input signal and the second input signal are an in-phase signal and a quadrature-phase signal respectively.

Claim 64 (new): The method of claim 63, wherein the first input signal and the second input signals are clock signals.

Claim 65 (new): The method of claim 63, wherein the first input signal and the second input signal are RF signals.

Claim 66 (new): The method of claim 63, wherein the first variable capacitor and the second variable capacitor are voltage-controlled capacitors.

Claim 67 (new): The method of claim 66, wherein the voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

Claim 68 (new): The method of claim 66, wherein the voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.